THAT WHICH IS CLAIMED IS:

1. A method of testing a sequential access memory plane adapted to store p words each of n bits, in which method p test words each made up of n test bits (DT) are written in the memory plane, the p test words are extracted from the memory plane, and the test bits of the extracted words are compared with expected binary data bits (DAi), characterized in that the p test words are extracted sequentially and, for each current word extracted, the n test bits that compose it are compared sequentially with n respective expected data bits (DAi) before extracting the next test word.

2. A method according to claim 1, characterized in that the p test words each of n bits are written in such a way as to obtain a checkerboard test binary configuration in the memory plane and in that the expected data is obtained sequentially from respective logical combinations of the read addresses (ai) of the test words and the ranks (rgi) of the test bits in each word that is read.

3. A sequential access semiconductor memory device including a memory plane (PMM) adapted to store p words each of n bits and test logic connected to the n outputs of the memory plane and including first test means (MT1) adapted to write into the plane p test words each composed of n test bits and second test means adapted to extract the p test words from the memory plane and compare the test bits of the extracted words with expected binary data bits, characterized in that the second test means are adapted to extract the p test words sequentially and, for each current extracted word, sequentially compare the n respective test bits that compose it with n expected data bits, before extracting the next test word.

4. A device according to claim 3, characterized in that the second test means include:

- a set of n chained output registers (BCi) connected to n respective outputs of the memory plane,
- first control means (MCD) adapted to deliver a first control signal (CB) to the n output registers so as to store simultaneously in those n registers the n test bits of the current test word,
- second control means (MCD) adapted to deliver to the n output registers a second control signal (CB) so as to shift the test bit contained in a register of the chain sequentially toward the next register and to extract sequentially from the register at the end of the chain the n test bits of the current test word, and
- comparator means (PL2) adapted to compare each bit extracted from said register at the end of the chain with the corresponding expected data bit.

5. A device according to claim 4, characterized in that each output register (BCi) is a D-type flip-flop having a data input (D) connected to one of the n outputs of the memory plane, a test input (TI), a test output (SO) and a test control input (TE) for receiving successively and alternately the first control signal and the second control signal (CB), the test output of a flip-flop is connected to the test input of the adjacent flip-flop to form said chain, the test input of the first flip-flop of the chain is adapted to receive an initial data bit (DDI), and the test output of the last flip-flop is connected to a first input of the comparator means.

6. A device according to claim 5, characterized in that the comparator means (PL2) include an EXCLUSIVE OR logic gate.

7. A device according to any of claims 3 to 6, characterized in that the first test means are adapted to write the p test words each of n bits in such a manner as to obtain in the memory plane a checkerboard test binary configuration and the test logic includes generator means (M1, CT) adapted to generate the expected data bits sequentially from respective logical combinations of the read addresses of the test words and the ranks of the test bits in each word that is read.

8. A device according to claim 7, characterized in that the generator means include:

- first means (M1) adapted to deliver the least significant bit of each read address,
- a counter (CT) adapted to contain a binary word representative of the rank of a test bit in the current word extracted from the memory plane,
- second means adapted to deliver the least significant bit of each binary word containing the counter, and
- an EXCLUSIVE OR logic gate (PL1) with two inputs connected to respective outputs of said first and second means and whose output delivers said expected data bits sequentially.